



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Modelski

Serial No.: 09/741857

Filed: 12/22/2000

Title: Multi-thread Packet Processor

Attorney Docket No.: 120-100

Group Art Unit:

2631

Examiner:

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JUL 16 2004

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Technology Center 2600

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This Information Disclosure Statement is submitted:

X under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of international application; or before mailing date of first office action on the merits; whichever occurs last)

X Applicant(s) submit herewith Form PTO 1449-Information Disclosure Citation together with copies, of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

The relevance of the attached references is that this is the closest art of which Applicant is aware. Applicant submits that the above references taken alone or in combination neither anticipate nor render obvious the present invention. Consideration of the foregoing in relation to this application is respectfully requested.

It is requested that the information disclosed herein be made of record in this application.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or the correspondence is being facsimile transmitted to the USPTO, on the date indicated below.

Date of Deposit: July 12, 2004

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Carol Ann Mahoney

Respectfully submitted,

H. W. Anderson

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Attorney/Agent for Applicant(s)

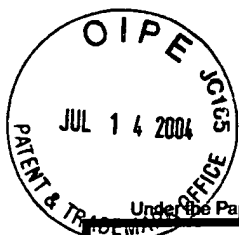
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PTO/SB/08a (08-03)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Complete if Known

Application Number	09/741857
Filing Date	12/22/2000
First Named Inventor	Modelski
Art Unit	2631
Examiner Name	
Attorney Docket Number	120-100

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
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FOREIGN PATENT DOCUMENTS

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		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
		WO00/70482A	23-11-2000	XStream Logic, Inc.		
		Copy of European Search Report 10.05.04 for 01310671.1-2211				

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Vibhatavanij, K. et al., "Simultaneous Multithreading-based Routers", Proceedings to the 2000 International Conf. on Parallel Processing; 21 Aug. 2000, pages 362-369	
		Eggers S.J. et al., "Simultaneous Multithreading: A Platform for Next-Generation Processors" IEEE Micro, IEEE Inc. New York, US, Vol. 17, no. 5, 1 September 1997, pages 12-19	
		Chang A. et al., "The Effects of Explicitly Parallel Mechanisms on the Multi-ALU Processor Cluster Pipeline" Computer Design: VLSI In Computers and Processors, 1998, ICCD '98, Proceedings, International Conference on Austin TX, Oct 5-7, 1998	

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